Mentor Forum 2019

New Era of IC to Systems Design

Mentor
A Siemens Business

AGENDA

09:00-10:00	등록 및 웰컴커피, 데모부스 관람
10:00-10:10	Welcome Speech
10:10-10:45	Keynote I: Semiconductor Design in the Machine Learning Era | Joe Sawicki, Executive VP, Mentor IC EDA, Mentor, a Siemens Business
10:45-11:20	Keynote II: Near Data Processing again in the Era of Data Explosion | Eui-Cheol Lim, Ph.D., Research Fellow, Memory System Architect, SK hynix
11:20-11:55	Keynote III: Image Analysis AI Technology and Its Applications | Jung-Bae Kim, Ph.D., CEO, Alchera
12:00-13:00	점심식사 및 데모부스 관람

	Track 1 IoT	Track 2 Electronic Board System	Track 3 Automotive IC	Track 4 Complex SoC	Track 5 Advanced Semi
13:00-13:45	Automated Formal Apps for SoC Verification Joon Hong	Automation of PCB Design verification using HyperlynxDRC Custom Rule Samsung : Minkyu Shim & Hyunjae Kim, Mentor : Ryan Chang	Mentor Safe IC - End-to-end Functional Safety Solution addressing ISO-26262 and ISO-21448 Ann Keffer	Leveraging HLS IP and Reference Designs to Accelerate AI and Image /Signal Processing Ansun Jeong	How to Reduce DRC Closure Time Enabling Faster SOC Tapeouts Hoonkoo Lee
13:45-14:30	Solido Solutions - Delivering Variation Aware Design and Characterization Powered by Machine Learning. Sungyoun Lee	New Electrical Design Best Practice or System Design and Analysis Andrew Kim	Plan Driven and Requirements Driven Verification Ann Keffer	A Metrics-Driven Power Methodology and SoC/ASIC Power for Real-World Scenarios Using Emulation Minsub Byun IP Development methodology on Veloce HYCON Samsung: Hyunjae Woo Mentor : YoungMin Jin	Calibre and the Cloud: Unlocking Massive Scaling MS Azure : Andy Chan Mentor : Jihun Park
14:30-14:50	커피 브레이크 및 데모부스 관람				
14:50-15:35	Addressing nm Mixed-Signal Verification Challenges with Symphony – Powered by the AFS Platform YuLing Lin	True Advanced Heterogeneous 3D IC-Package Verification & Implementation Rock Kim	The PAVE360 Program offers Chip-to-Vehicle verification continuity methods combining electronics, sensors and powertrain modeling for faster development of Safer Autonomous Vehicles Gabriele Pulini	Plug and Play SoC DFT architecture Wu Yang	Calibre LVS: Innovation beyond a Verification Flow; A Complete Platform to Downstream Tools Charles Jung
15:35-16:20	Predicting Silicon Performance with High Accuracy Parasitic Extraction Sean Byun	ECAD-MCAD Co-design/Collaboration with cross probing across domains. Mentor : Sanghoon Lee Siemens Digital Industry Software : HeeSong Noh	Automotive DFT platform for highly reliable SoC Samsung : Yoseop Lim Mentor : Inchul Kim	UVM and Portable Stimulus: A Match Made in Heaven Sungjin Park	Calibre PERC: Sign-Off Solutions for Circuit Reliability Jaeman Jung
16:20-16:30	맺음말 및 경품 추첨				

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